SC8915 EVM USER GUIDE

——Southchip Semiconductor

1 Fundamental Information

SC8915 EVM board is used for Buck-Boost controller SC8915 which is featured with high efficiency, bi-direction operation and integrated I2C interface. User can configure parameters flexibly through I2C interface on the SC8915 EVM board. Besides, the charging/discharging function and all chip performance can be evaluated with EVM board.

SC8915 EVM board parameters are as follow:

Table 1. SC8915 EVM parameter

EVM board version	SC8915_EVM_C13.1
Support charging/discharging bi-direction operation	Yes
Support Buck and Boost	Yes
Integrated MOSFET	Yes
Support I2C interface	Yes
Support power path management	Yes
Smart detection function	Adapter insertion detection Load insertion detection
ADC resolution	10 bits
VBUS operation range in charging mode	2.7~36V
VBAT operation range in charging mode	2.7V~36V (default: 4.2V, configured by I2C)
VBAT operation range in discharging mode	2.7~36V
VBUS operation range in discharging mode	2.7V~36V (default: 5V, configured by I2C)
Inductor peak current IL	15A
Maximum input/output average current(IBUS)	6A@10mΩconfigured by I2C
Maximum input/output average current(IBAT)	12A @10mΩ configured by I2C
IBUS current sense resistor value	10mΩ
IBAT current sense resistor value	10mΩ /5mΩ
Switching frequency	150kHz/300kHz(default)/450kHz, configured by I2C
Discharging efficiency (VBAT=7.2V, VBUS=5V, IBUS=2.4A)	96%

VBUS capacitor	50V/10μF x 6
VBAT capacitor	50V/10μF x 6
EVM board dimension	56.5mm x 41.9mm (4-layer board)

2 Interface and I2C configurations

2.1 Input/output interface

Table 2 shows input/output interface functions and configurations:

Table 2. EVM Interface function description

Designator	Name	Description
J1	VBUS	VBUS terminal, as input in charging mode, output in discharging mode
J2	GND	Power ground of USB port
J3	VBAT	VBAT terminal, connected to battery, as output in charging mode, input in discharging mode
J4	GND	Power ground of battery port
J5	USB1	Micro USB adapter input port, isolated with VBUS by Q1 MOSFET
J6	USB2	USB-A output port, isolated with VBUS by Q4 MOSFET
P2	USB2-DRV	P2 interface's middle pin is USB2_DRV, which is useless default. If using this pin, R31 should be removed and R13 will be 0R. So, USB2_DRV is driver signal of Q4 MOSFET between USB2 port and VBUS port. 1, If USB2_DRV is connected with Low (left pin), the Q4 will be closed. 2, If USB2_DRV is connected with High (right pin), the Q4 will be opened.
P3	I2C/INT	P1 interface pins are SCL/SDA/V3P3/AGND/INT from left to right respectively. SCL/SDA is I2C communication interface; V3P3 is 3.3V pull-up power (provided by external power, if I2C tool is connected with computer, the power will be provided by computer); AGND is analog ground; INT is interrupt signal.
P4	PSTOP	The middle pin of P6 interface is PSTOP, PSTOP is chip power control signal. 1. If PSTOP is floating or connected with AGND (right pin), power module is enabled. 2. if PSTOP is connected to VHI (left pin), power module is disabled.
P5	AGND	Analog ground.
P6	ADIN	ADIN lies on the right pin of P4. ADIN is analog input port of 10 bits ADC, and the full amplitude is 2.048V; if ADC is disabled, it's suggested that

		ADIN is connected with AGND (the left pin of P4).

2.2 Test Point

Table 3 shows test point.

Table 3. Test point description

Designator	Name	Description
TP1	USB1	MicroUSB port USB1 test point
TP1	USB2	USB-A port USB2 test point
TP3	SW1	Switching node 1 test point
TP4	SW2	Switching node 2 test point

2.3 I2C Configuration

SC8915 has an I2C control interface. The user can configure charging/discharging operation, switching frequency, charging target voltage, input regulation voltage (VINREG) in charging mode; VBUS voltage in discharging mode; IBUS limit current; IBAT limit current and so on. The User can also control power path and read various protective states and intelligent detection states through I2C interface. In addition, chip's integrated ADC function also needs to be turned on through the I2C, and the data of the ADC conversion are also stored in the registers.

The device address is 0x74 (7bits). The following is a brief introduction of setting voltage/current and read voltage/current through I2C interface, and the specific register table can be referred to **SC8915** datasheet.

2.3.1 SouthChip I2C GUI Tool Guidance

I2C GUI Tool is developed by **SouthChip**, convenient for customers to debug.

When VBUS is decided by external configuration, the Rup and Rdown values marked with red color on the lower part of the interface should be filled according to the actual resistance on EVM. In this way, the voltage value shown in blue marker 1 is the true VBUS voltage value.

In the same way, if user fills the current sense resistance values of IBUS (RS1) and IBAT (RS2) on the EVM in the RS1 and RS2 marked with red color, then the I2C GUI will show the actual IBUS_LIM and IBAT_LIM set values, as well as real-time value of IBUS and IBAT.

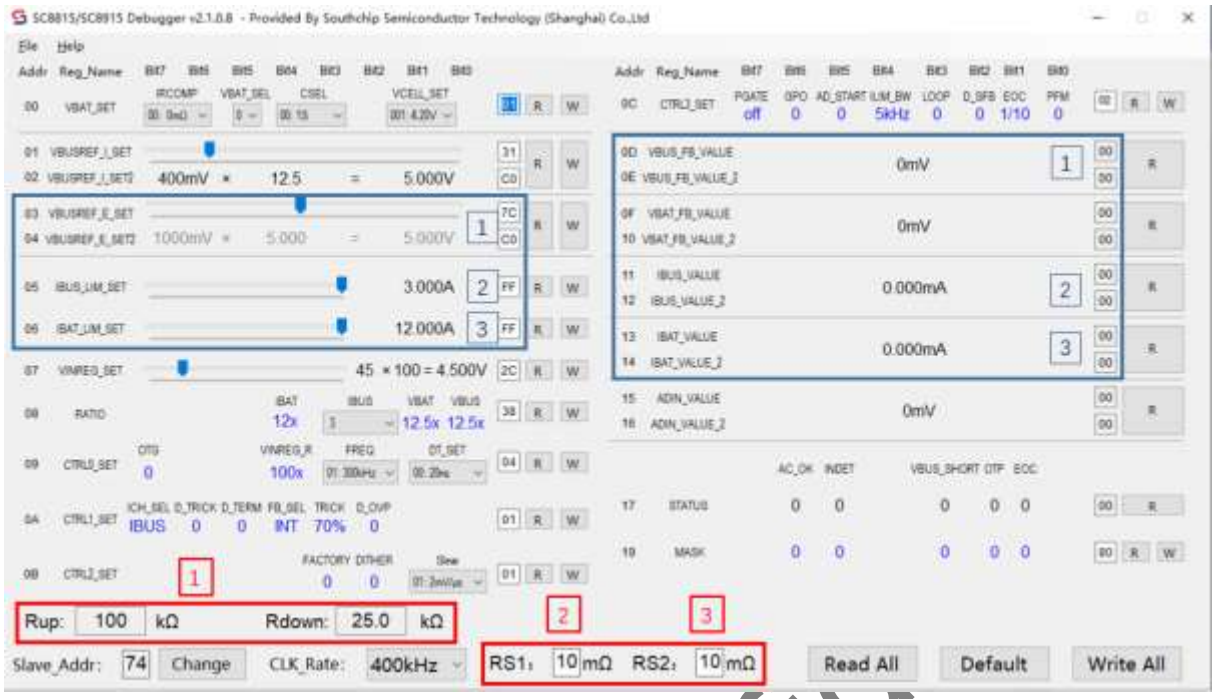


Figure 1 SC8915 I2C tool interface

2.3.2 Charging Target Voltage in Charging Mode

Firstly, set Reg 0x09<7> (**OTG_EN**) =0 to work in charging mode.

a) Charge target voltage VBAT is decided by internal setting

VBATS pin should be connected with VBAT network and set Reg 0x00<5> (**VBAT_SEL**) =0.

CSEL: Reg 0x00<4:3>, used to set battery cell numbers

VCELL_SET: Reg00<2:0>, used to set target cell voltage value

The default charge target voltage value for each cell is 4.2V. User can configure it from 4.1V to 4.5V

b) Charge target voltage is decided by external setting

VBATS should be connected with resistor divider of VBAT and set Reg 0x00<5> (**VBAT_SEL**) =1. The reference voltage **VBATS_REF** is constant 1.2V.

$$VBAT = V_{BATS\_REF} \times \left(1 + \frac{R_{UP}}{R_{DOWN}}\right)$$

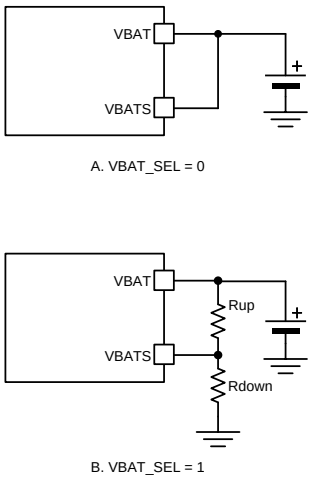


Figure 2 SC8915 charge target voltage setting circuit

What's more, **SC8915** integrates battery impendence compensation function, no matter internal or external configuration. Reg 0x00<7:6>(**IRCOMP**) is used to set compensation voltage.

So the real target voltage can be calculated as follow:

$$VBAT\_cmp = VBAT\_set + \min(IBAT \cdot IRCOMP, VCLAMP)$$

VCLAMP is the allowed maximum compensation value, fixed at 125mV.

Table 4. VBAT_SEL Reg table

Bit	Mode	Bit Name	Default value @POR	Description
7-6	R/W	IRCOMP	00	Battery IR compensation setting: 00: 0 mΩ (default) 01: 20 mΩ 10: 40 mΩ 11: 80 mΩ
5	R/W	VBAT_SEL	0	VBAT voltage setting selection: 0: internal setting (default) 1: external setting
4-3	R/W	CSEL	00	Battery cell selection, only valid for internal VBAT voltage setting 00: 1S battery (default) 01: 2S battery 10: 3S battery 11: 4S battery
2-0	R/W	VCELL_SET	001	Battery voltage setting per cell, only valid for internal VBAT voltage setting 000: 4.1V 001: 4.2V (default) 010: 4.25V

				011: 4.3V 100: 4.35V 101: 4.4V 110: 4.45V 111: 4.5V

2.3.3 VBUS Output Voltage Setting in Discharging Mode

Firstly, set Reg bit 0x09<7> (OTG_EN) =1 to operate in discharging mode.

a) VBUS is decided by internal setting

FB should be floating and set Reg 0x0A <4> (FB_SEL) =0.

VBUS output voltage is decided by **VBUSREF_I_SET**, **VBUSREF_I_SET2**, and **VBUS_RATIO**.

VBUSREF_I_SET: Reg 0x01<7:0>

VBUSREF_I_SET2: Reg 0x02<7:6>

VBUS_RATIO: Reg 0x08<0>

The internal reference voltage can be calculated as follow:

VBUSREF_I = (4 x VBUSREF_I_SET + VBUSREF_I_SET2 + 1) x 2 mV

The recommended VBUS voltage range is from 3.5V to 25.6V.

- When VBUS is lower than 10.24V, it is suggested to set the **VBUS_RATIO** to 5x, and so the minimum changing step is 10mV/step;
- When VBUS is higher than 10.24V, **VBUS_RATIO** should be set to 12.5x, and the minimum changing step is 25mV/step.

VBUS voltage can be calculated as below:

VBUS = VBUSREF_I x VBUS_RATIO

b) VBUS is decided by external setting

Set Reg 0x0A <4> (**FB_SEL**) =1 and FB pin should be connected with resistor divider of VBUS.

The VBUS external reference voltage is decided by **VBUSREF_E_SET** and **VBUSREF_E_SET2**.

VBUSREF_E_SET: Reg 0x03<7:0>

VBUSREF_E_SET2: Reg 0x04<7:6>

The VBUS external reference voltage can be calculated as below. The adjustable reference voltage range is 0.7V~2.048V, the default value is 1V.

VBUSREF_E = (4 x VBUSREF_E_SET + VBUSREF_E_SET2 + 1) x 2 mV

VBUS voltage can be calculated as below:

$$VBUS = VBUSREF\_E \times (1+\frac{RUP}{RDOWN})$$

External setting is chosen as the default configuration on the EVM board. R27(RUP) value is 100kΩ, R28(RDOWN) value is 24kΩ, so the default output voltage of VBUS is 5.17V.

Note: If more accurate voltage value is needed, 0.1% accuracy resistor is suggested.

2.3.4 IBUS Current Limit Setting

IBUS current limit function is effective in both charging and discharging mode.

IBAT current limit is decided by **IBUS_LIM_SET** and **IBUS_RATIO**.

IBUS_LIM_SET: Reg 0x05<7:0>

IBUS_RATIO: Reg 0x08<3:2>

- When Reg 0x08<3:2> (IBAT_RATIO) =01, IBUS_RATIO=6;
- When Reg 0x08<3:2> (IBUS_RATIO) =10, IBUS_RATIO=3;

RS1 is the IBUS sense resistor value.

$$\text{IBUS\_LIM (A)} = \frac{(\text{IBUS\_LIM\_SET} + 1)}{256} \times \text{IBUS\_RATIO} \times \frac{10\ \text{m}\Omega}{\text{RS1}}$$

RS1 value is 10mΩ, the default IBUS current limit is 3A.

2.3.5 IBAT Current Limit setting

IBAT current limit function is effective in both charging and discharging mode.

IBAT current limit is decided by: **IBAT_LIM_SET** and **IBAT_RATIO**.

IBAT_LIM_SET: Reg 0x06<7:0>

IBAT_RATIO: Reg 0x08<4>

- When Reg 0x08<4> (IBAT_RATIO) =0, IBUS_RATIO=6;
- When Reg 0x08<4> (IBAT_RATIO) =1, IBUS_RATIO=12.

RS2 is the IBAT sense resistor.

$$\text{IBAT\_LIM (A)} = \frac{\text{IBAT\_LIM\_SET}+1}{256} \times \text{IBAT\_RATIO} \times \frac{10\ \text{m}\Omega}{\text{RS2}}$$

RS2 value is 5mΩ, the default IBUS current limit is 24A.

2.3.6 VINREG Setting

During charging, if the IBUS charging current is higher than adapter's current capability, the adapter will be overloaded and the VBUS voltage is pulled low. Once the IC detects the VBUS voltage drops at VINREG threshold, it reduces the charging current automatically and regulates the VBUS voltage at VINREG threshold.

VINREG value is decided by: **VINREG_SET** and **VINREG_RATIO**.

VINREG_SET: Reg 0x07<7:0>

VINREG_RATIO: Reg 0x09<4>

- When Reg 0x09<4>=0, VINREG_RATIO=100.
- When Reg 0x09<4>=1, VINREG_RATIO=40 (Suit for VINREG<10V).

$$\text{VINREG} = (\text{VINREG\_SET}+1) \times \text{VINREG\_RATIO}\ \ (\text{mV})$$

2.3.7 ADC Setting

SC8915 provides 5-channel ADC sampling for VBUS/VBAT/IBUS/IBAT/ADIN. Set Reg 0x0C<5> (ADC_START) =1 to enable ADC function.

a) VBUS value can be calculated by **VBUS_FB_VALUE** and **VBUS_FB_VALUE2**:

VBUS = (4 x VBUS_FB_VALUE + VBUS_FB_VALUE2 + 1) x VBUS_RATIO x 2 mV

VBUS_FB_VALUE: set by Reg 0x1D<7:0>

VBUS_FB_VALUE2: set by Reg 0x0E<7:6>

b) VBAT value can be calculated by **VBAT_FB_VALUE** and **VBAT_FB_VALUE2**:

VBAT = (4 x VBAT_FB_VALUE + VBAT_FB_VALUE2 + 1) x VBAT_MON_RATIO x 2 mV

VBAT_FB_VALUE: set by Reg0x0F<7:0>

VBAT_FB_VALUE2: set by Reg0x10<7:6>

- When Reg 0x08<1> (**VBAT_MON_RATIO**) =0, VBAT_MON_RATIO=12.5(default);
- When Reg 0x08<1> (**VBAT_MON_RATIO**) =1, VBAT_MON_RATIO=5. For 1~2 cell application, it's suggested to choose VBAT_MON_RATIO=5.

c) IBUS value can be calculated by **IBUS_VALUE** and **IBUS_VALUE2**:

$$IBUS\ (A) = \frac{(4 \times IBUS\_VALUE + IBUS\_VALUE2 + 1) \times 2}{1200} \times IBUS\_RATIO \times \frac{10\ m\Omega}{RS1}$$

IBUS_VALUE: set by Reg 0x11<7:0>

IBUS_VALUE2: set by Reg 0x12<7:6>

d) IBAT value can be calculated by **IBAT_VALUE** and **IBAT_VALUE2**:

$$IBAT\ (A) = \frac{(4 \times IBAT\_VALUE + IBAT\_VALUE2 + 1) \times 2}{1200} \times IBAT\_RATIO \times \frac{10\ m\Omega}{RS2}$$

IBAT_VALUE: set by Reg 0x13<7:0>

IBAT_VALUE2: set by Reg 0x14<7:6>

e) VADIN value can be calculated by **ADIN_VALUE** and **ADIN_VALUE2**:

VADIN = (4 x ADIN_VALUE + ADIN_VALUE2 + 1) x 2 mV

ADIN_VALUE: set by Reg 0x15<7:0>

ADIN_VALUE2: set by Reg 0x16<7:6>

Note: when the chip is set as standby mode (PSTOP = H), user shall set the Reg 0x0C<5> (ADC_START) to 0 to disable ADC function, reducing the quiescent current.

2.4 Other Settings

2.4.1 Loop compensation setting

COMP pin is used for loop compensation setting. R25=10kΩ and C28=22nF is suggested for typical application.

Once loop instability occurs, R25 and C28 should be adjusted according to practical situation.

2.4.2 MOSFET driver resistor setting

R9/R10 is driver resistor which connects LD/HD with LG/HG respectively on the EVM board. The default value of R9/R10 is 0 ohm. Increasing R9/R10 value will slow down switching speed and improve EMI performance, but with the cost of decreased efficiency at the same time.

2.4.3 Power path management Q2/Q4 driver setting

Q2/Q4/Q1 is the power MOSFET used to control the power path. Q2's driver signal is connected to GPO pin; Q4's driver signal is connected to PGATE pin; Q1's driver signal is connected to MicroB_drv pin(P5);

Through I2C interface, Q4 and Q2 can be controlled by 0x0C<7> (EN_PGATE) and 0x0C<7> (GPO_CTRL) respectively. When the corresponding setting bit is 1, Q4/Q2 will be on. Otherwise, Q4/Q2 will be off. Specification description can be referred to **SC8915** datasheet.

2.4.4 Adapter Attachment/Detachment Detection

MicroUSB adapter attachment/detachment detection is realized by ACIN pin. When chip detects adapter plug-in, it will set AC_OK interrupt bit, and INT pin will assert interrupt signal. Specification description can be referred to **SC8915** datasheet

2.4.5 Dithering function test configuration

If switching frequency dithering function is tested, R17 should be removed and USB2 should disconnected. R15 value is set to 0 ohm, PGATE/DITH pin will be used for frequency dithering.

3 Test Precautions

1) When USB2 is used as output port, Register need be configured to open MOS Q4. When USB1 is used as output port, Register need be configured to open MOS Q1.

2) If power path function is not tested, USB interface can be always connected to VBUS port , battery can be connected to VBAT port. Chip operation mode can be changed by EN_OTG bit.

3) In the charging mode, USB charges the battery from VBUS to VBAT; in the reverse discharging mode, battery discharges power from VBAT to VBUS.

4) PSTOP and /CE pin should be floating or connected to ground to enable the power operation.

5) It's suggested to start up with no load or CR mode electronic load. Load can't be so heavy that exceeds the current limit of SC8915, or it can not start up normally.

6) After starting up, if the electronic load CC mode is used as the load, it should be noted that the CC load current should not exceed the output current limit, and the corresponding input current should not exceed the input current value. Otherwise, the CC load will pull the output voltage down directly. If CR mode loading is used, even if the input / output current limit occurs, the output voltage still can be stabilized at a balance point and will not be forced down.

4 EVM Schematic and BOM List

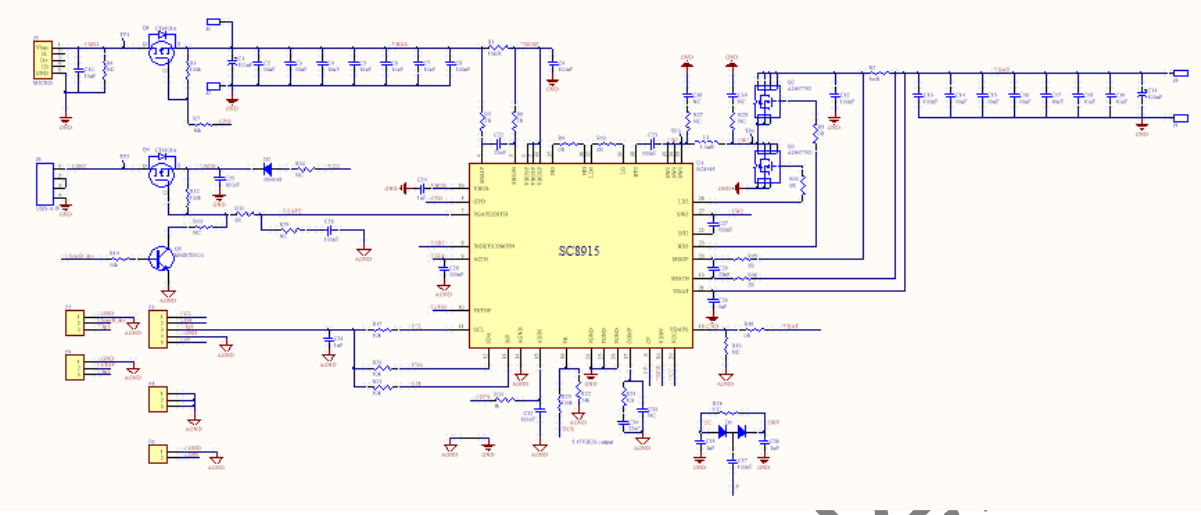


Figure 3 SC8915 EVM schematic

BOM list is as follow.

Table 5. SC8915 EVM BOM list

Reference	Description	Value	Part Number	Vendor	Quantity
C1, C11	POSCAP (Solid electrolytic capacitor), 6.3x11, 35V, 100uF	100uF/35V	std	std	2
C2, C3, C4, C5, C6, C7, C10, C14, C15, C16, C17, C18, C19	Capacitor, X5R, 1206, 50V, 10%, 10uF	10uF/50V	GRM31CB31H106KA12#	Murata	13
C8, C13	Capacitor, X5R, 0603, 50V, 10%, 100nF	100nF/50V	GRM319B11H104KA01#	Murata	2
C25, C28	Capacitor, X5R, 0402, 25V, 10%, 100nF	100nF/25V	GRM155R61E104KA87#	Murata	2
C23, C27, C37	Capacitor, X5R, 0603, 10V, 10%, 100nF	100nF/10V	GRM188R61C104KA01#	Murata	3
C26, C32	Capacitor, X5R, 0603, 6.3V, 10%, 100nF	100nF/6.3V	GRM188R61C104KA01#	Murata	2
C9, C12	Capacitor, X5R, 0402, 50V, 10%, 100nF	100nF/50V	std	Murata	2
C22, C29, C34	Capacitor, X5R, 0603, 6.3V, 10%, 22nF	22nF/6.3V	GRM188R61H223KA01#	Murata	3
C24, C30	Capacitor, X5R, 0603, 50V, 10%, 1uF	1uF/50V	GRM31MB31H105KA87#	Murata	2
C35, C36	Capacitor, X5R, 0603, 10V, 10%, 1uF	1uF/10V	GRM185R61A105KE26#	Murata	3

C31	Capacitor, X5R, 0603, 6.3V, 10%, 1uF	1uF /6.3V	GRM185R61A105KE26#	Murata	1
C33, C38, C39	Capacitor	NC	std	Std	3
D1	Dual_diode	100V0.2A	MMBD4148SE	Fairchild	1
D2	diode	1N4148	1N4148	Philips	1
J1, J2, J3, J4	Jack	JACK	std	std	4
J5		MICRO	std	std	1
J6		USB-A-H	std	std	1
L1	Inductor, 3.3uH, 13x13x5	Inductor	CMLB135T-3R3MS	Cyntec	1
P3	Header, 5-Pin	Header 5	std	std	1
P2, P4, P5	Header, 3-Pin	Header 3	std	std	3
P6	Header, 2-Pin	Header 2	std	std	1
Q1, Q4	30V PMOS, SOT23, CJ3401A /AO3401A/AO3401/VS3407A	CJ3401A	2N7002/MMBT3904	A&O	2
Q2, Q3	30V NMOS, 3*3, AON7752 /TDM3478 /PE616BA	NMOS_3*3	AON7752 /TDM3478 /PE616BA	A&O	2
Q5	NPN/NMOS, SOT23, MMBT3904/2N7002	MMBT3904	std	std	1
R1	Metal resistor, 1206, 1W, 1%	10mR	std	std	1
R2	Metal resistor, 1206, 1W, 1%	5mR	std	std	1
R3, R12,R25	Resistor, 0603, 1/4W, 1%	100k	std	std	3
R4, R13, R19, R26, R27, R28, R29, R30	Resistor, 0603, 1/4W, 1%	NC	std	std	8
R5, R6, R15, R16	Resistor, 0603, 1/4W, 1%	2R	std	std	4
R7, R14, R17, R20, R21, R23	Resistor, 0603, 1/4W, 1%	10k	std	std	6
R8, R9, R10, R11, R18, R31	Resistor, 0603, 1/4W, 1%	0R	std	Std	6
R22	Resistor, 0603, 1/4W, 1%	24k	std	std	1
R24	Resistor, 0603, 1/4W, 1%	1k	std	std	1

TP1, TP2, TP3, TP4	test point	TP	std	std	4
U1	Main IC	SC8915	SC8915	Southchip	1

5 PCB Layout

SC8915 EVM board PCB layout is as follow:

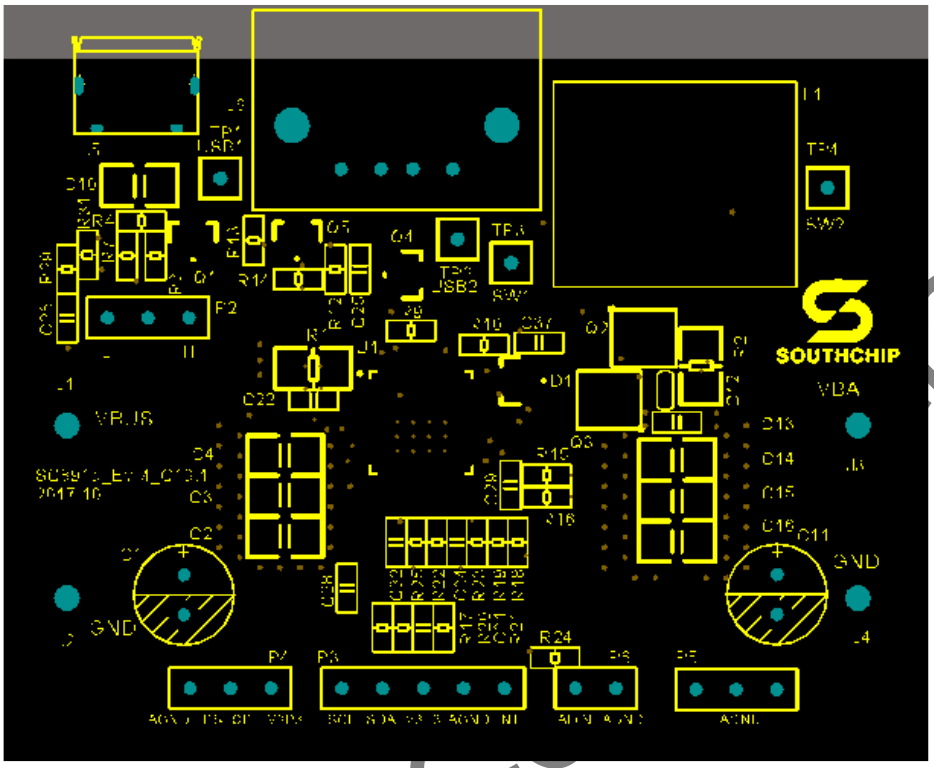


Figure 4 Top Silkscreen

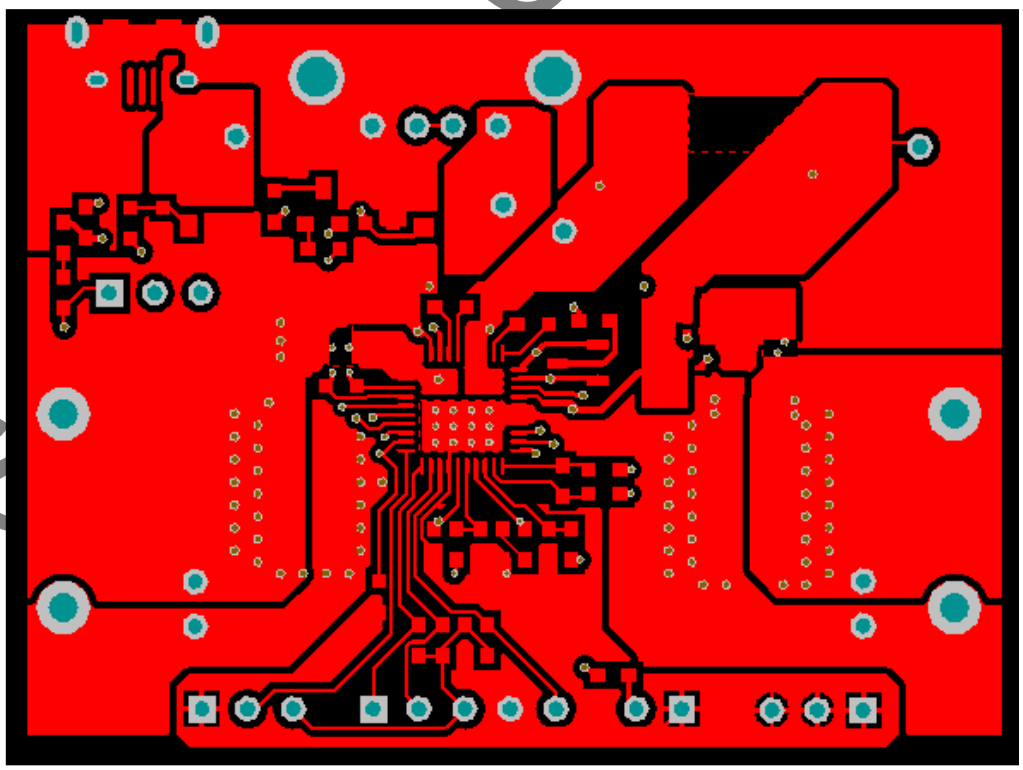


Figure 5 Top Layer

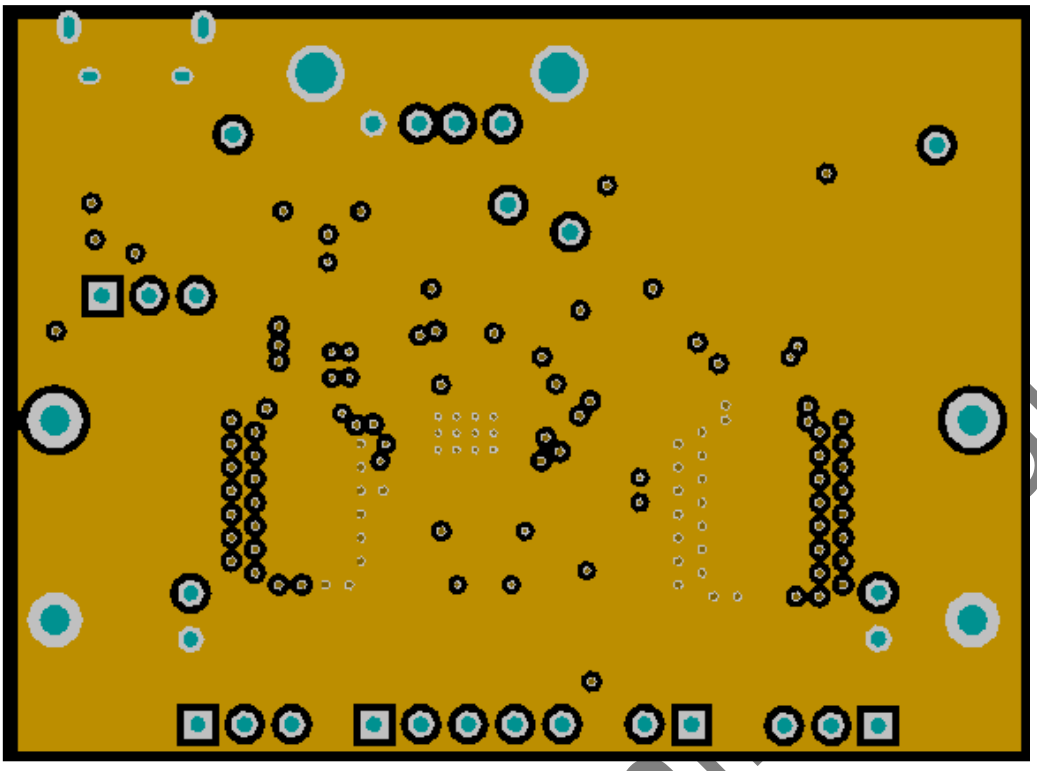


Figure 6 Mid Layer1

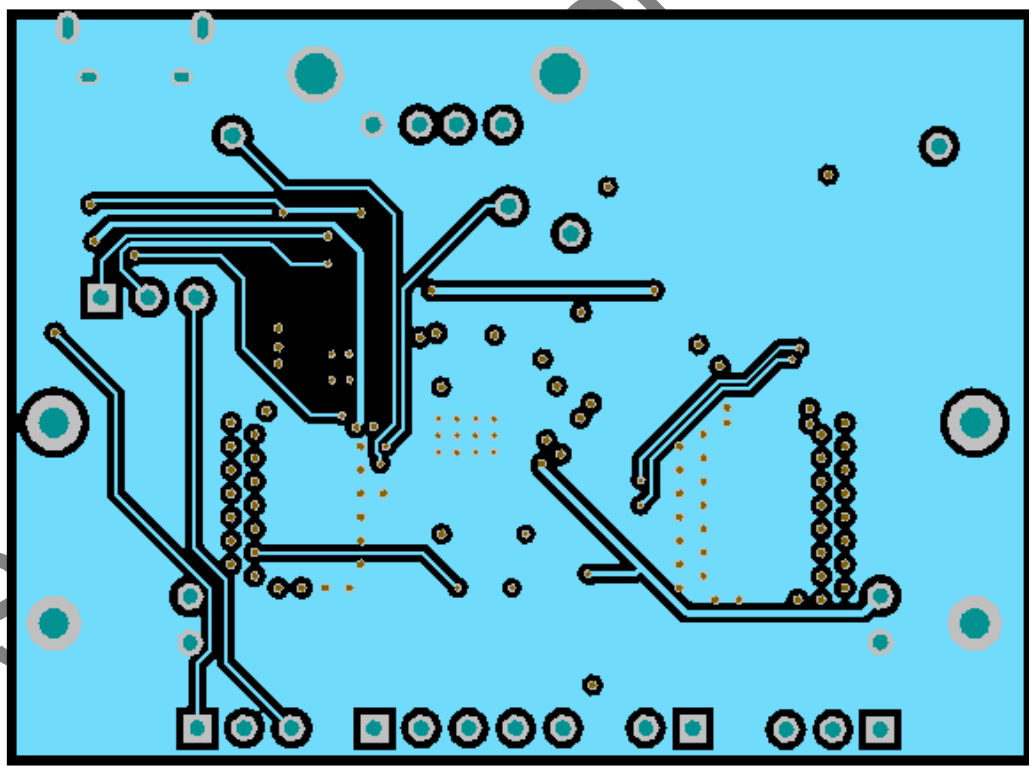


Figure 7 Mid Layer2

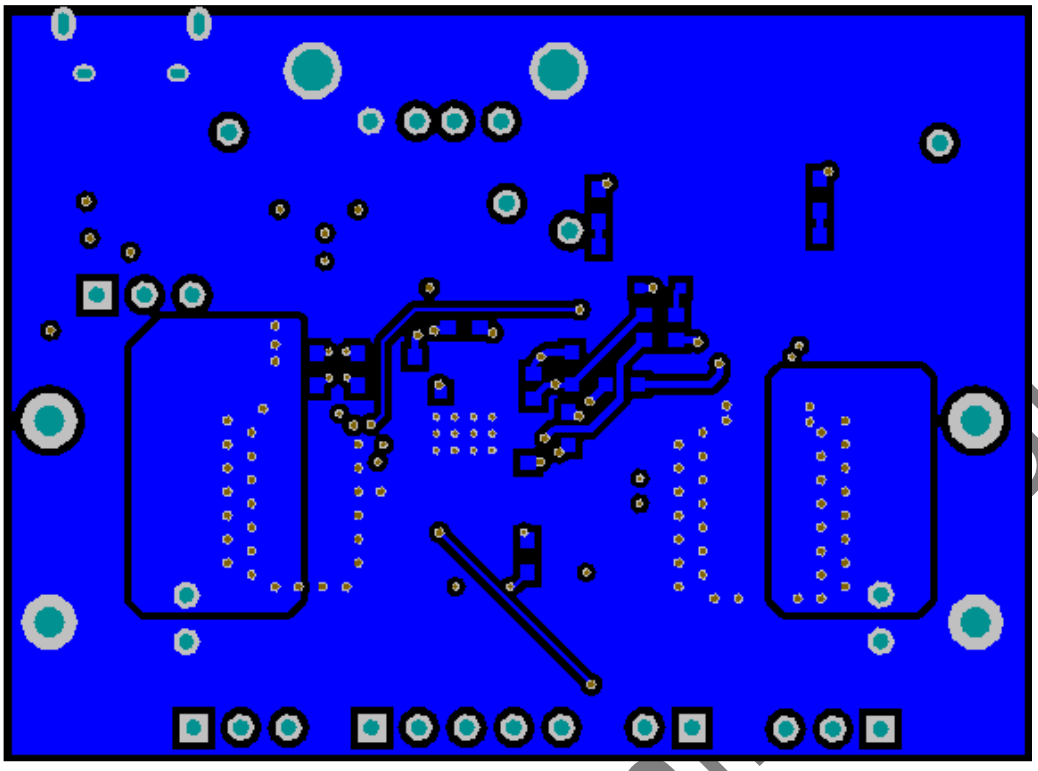


Figure 8 Bottom Layer

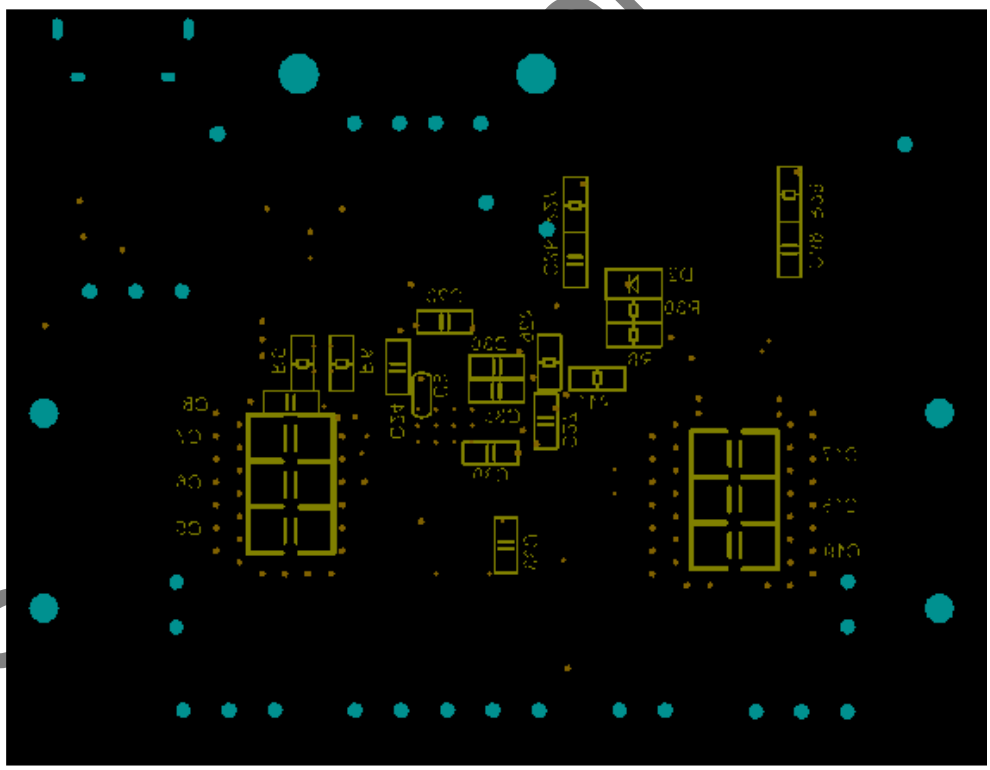


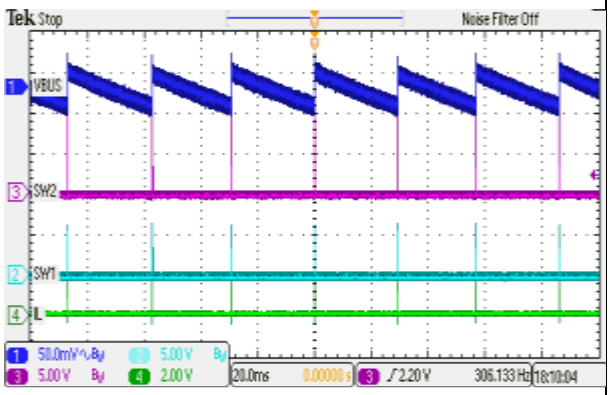
Figure 9 Bottom Silkscreen

6 Tested Data and Waveform

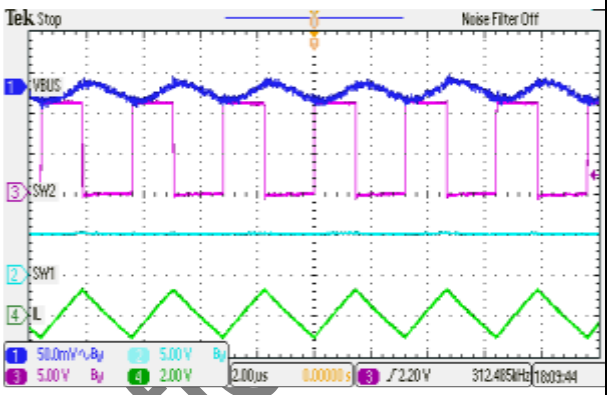
6.1 VBUS Output Voltage Ripple in Discharging Mode

fsw = 300kHz, L = 3.3uH, RS1 = 10mR, RS2 = 5mR, COMP = 10k + 22nF, VBAT=10.8V

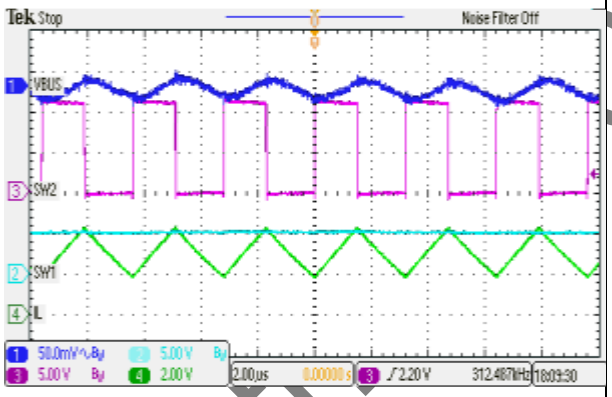
VBUS = 5V, IBUS= 0A, PFM



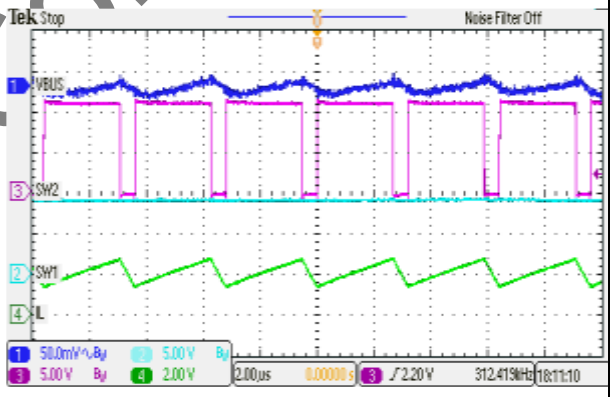
VBUS = 5V, IBUS= 0A, PWM



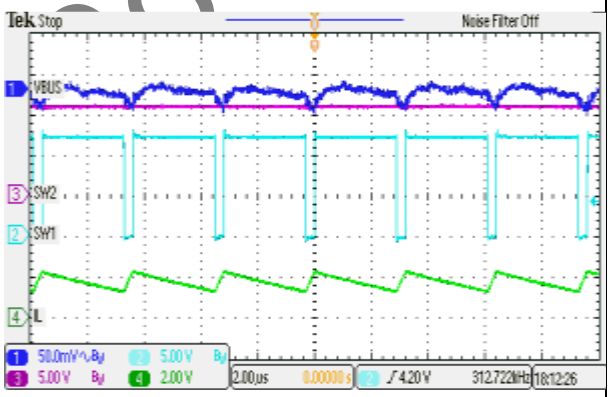
VBUS = 5V, IBUS= 3A



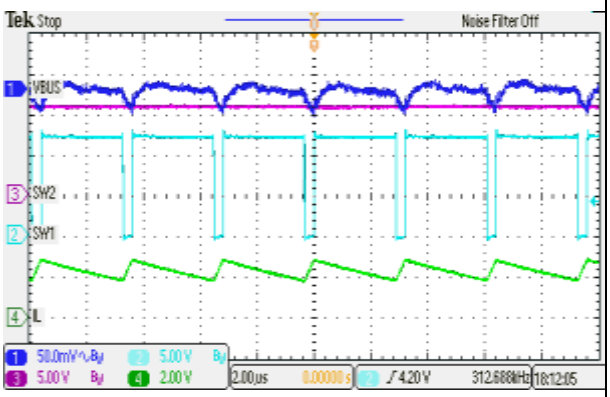
VBUS = 9V, IBUS= 2A



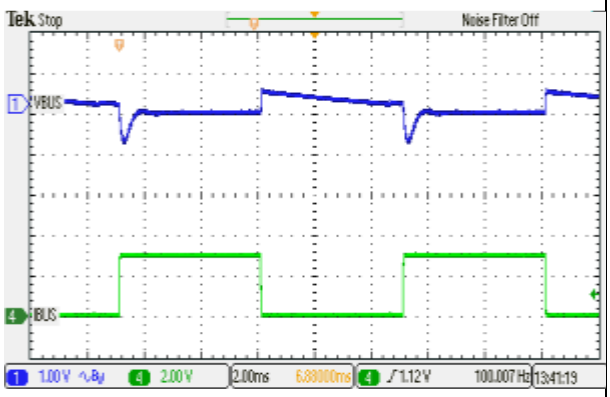
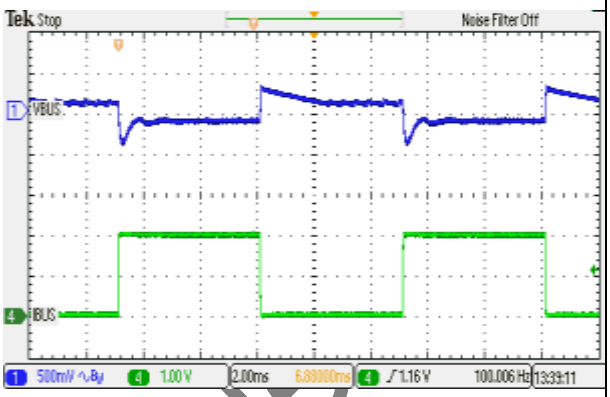
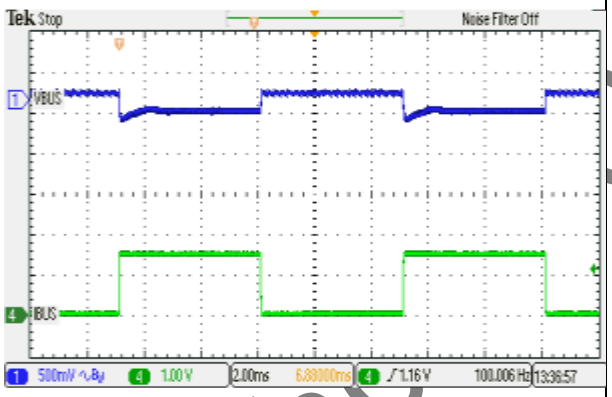
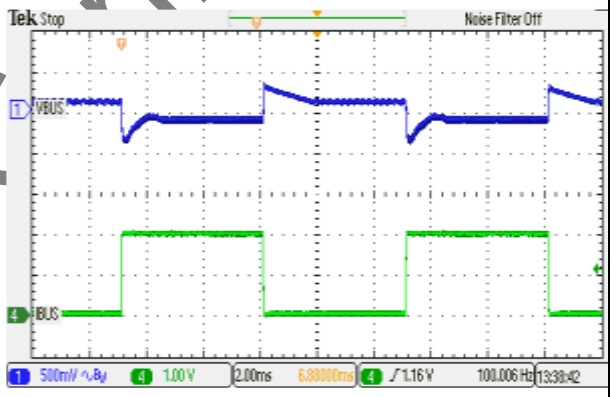
VBUS = 12V, IBUS= 1.5A



VBUS = 12V, IBUS= 2A

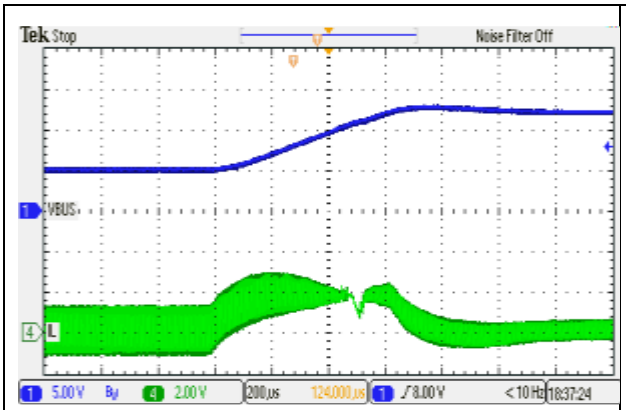


6.2 VBUS Waveform in Load Transition in Discharging Mode

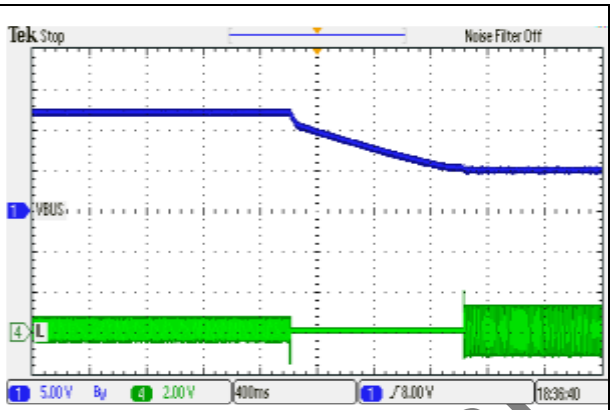
fsw = 300kHz, L = 3.3uH, RS1 = 10mR, RS2 = 5mR, COMP = 10k + 22nF, Loop bit=1, VBAT=10.8V, PFM	
VBUS = 5V, IBUS=0A~3A, Slew-Rate=1A/μs	VBUS = 9V, IBUS=0A~2A, Slew-Rate=1A/μs
	
VBUS = 12V, IBUS=0A~1.5A, Slew-Rate=1A/μs	VBUS = 12V, IBUS=0A~1.5A, Slew-Rate=1A/μs
	

6.3 VBUS Voltage Dynamic Scaling in Discharging Mode

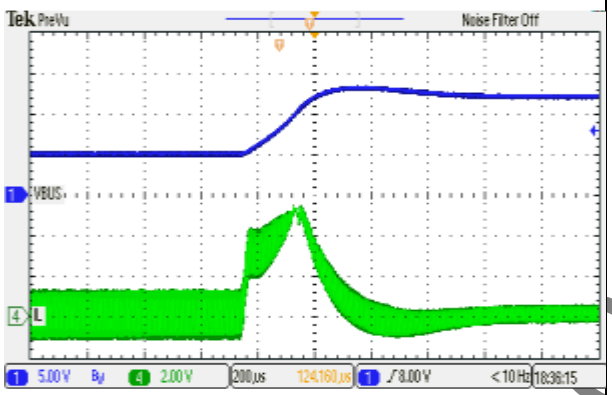
fsw = 300kHz, L = 3.3uH, RS1 = 10mR, RS2 = 5mR, COMP = 10k + 22nF, VBAT=10.8V	
IBUS=0A, VBUS = 5~12V, Slew-Rate=1mV/μs	IBUS=0A, VBUS = 12~5V, Slew-Rate=1mV/μs

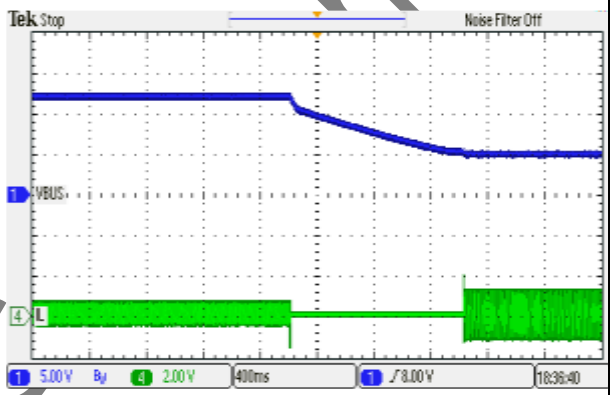


IBUS=0A, VBUS = 5~12V, Slew-Rate=8mV/uS



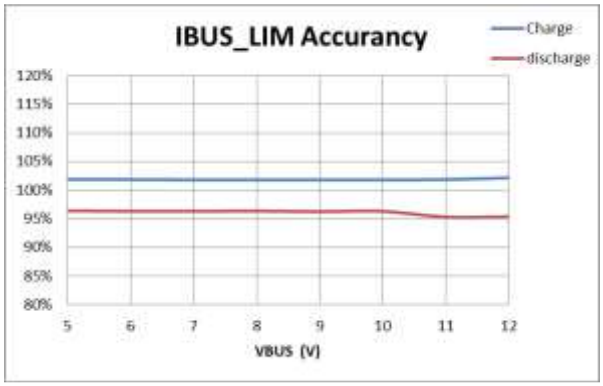
IBUS=0A, VBUS = 12~5V, Slew-Rate=8mV/uS

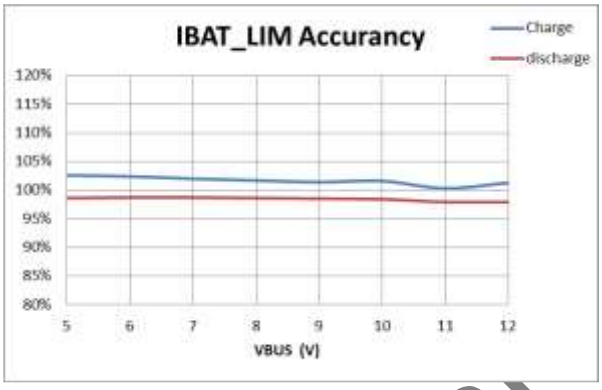




6.4 Current Limit Accuracy in Charging/Discharging mode

fsw = 300kHz, L = 3.3uH, RS1 = 10mR, RS2 = 5mR, COMP = 10k + 22nF, VBAT=10.8V	
Charge/discharge mode, VBUS = 5~12V, Set IBUS_LIM=2A	Charge/discharge mode, VBUS = 5~12V, Set IBAT_LIM=2A





6.5 Discharging Efficiency

fsw = 300kHz, L = 3.3uH, RS1 = 10mR, RS2 = 5mR, COMP = 10k + 22nF, PFM mode

VBAT= 7.2V, VBUS=5V/9V/12V

VBAT= 10.8V, VBUS=5V/9V/12V

VBAT= 14.4V, VBUS=5V/9V/12V

6.6 Supply Current

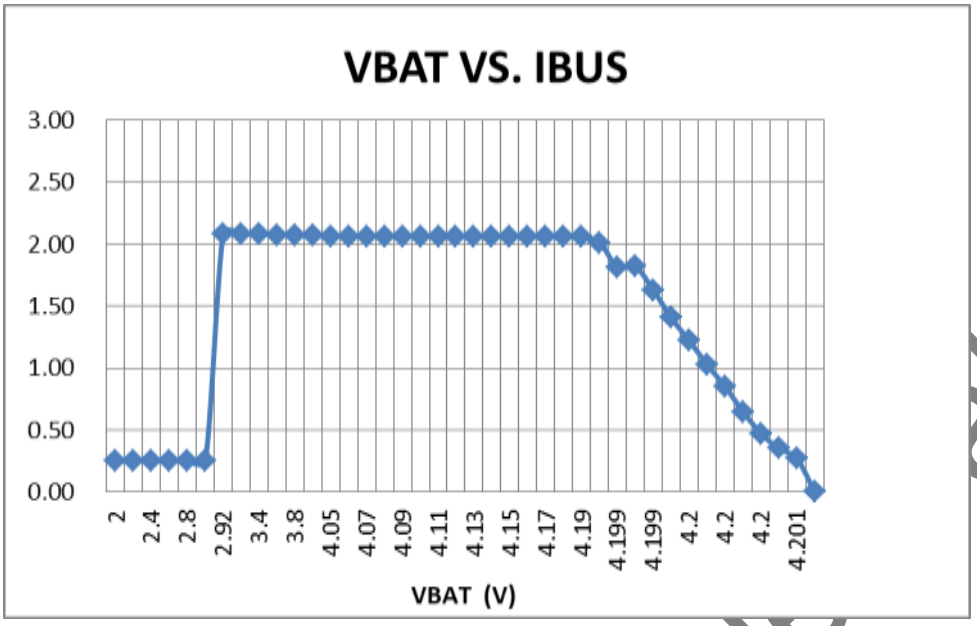
fsw = 300kHz, L = 3.3uH, RS1 = 10mR, RS2 = 5mR, COMP = 10k + 22nF, VBAT=10.8V	
Test Condition	Test Result
PSTOP=3.3V, VBUS floating, Measure current into VBAT, Board level, AD_START=1	I_SB_VBAT=25μA
PSTOP=3.3V, VBUS floating, Measure current into VBAT, Board level, AD_START=1	I_SB_VBAT_ADC=658μA

6.7 Temperature Rise Test in Discharging Mode

fsw = 300kHz, L = 3.3uH, RS1 = 10mR, RS2 = 5mR, COMP = 10k + 22nF, VBAT=10.8V	
Test Condition	Test Result
VBUS=5V, IBUS=3A, Temperature rise of IC/Q2/Q3 surface	T_RISE= 12 /10 /9 °C
VBUS=9V, IBUS=2A, Temperature rise of IC/Q2/Q3 surface	T_RISE= 9 /7 /8 °C
VBUS=12V, IBUS=2A, Temperature rise of IC/Q2/Q3 surface	T_RISE= 12 /7 /7 °C

6.8 Charging Curve

fsw = 300kHz, L = 3.3uH, RS1 = 10mR, RS2 = 5mR, COMP = 10k + 22nF
Charging mode, VBUS = 5V, Set IBUS_LIM=2A, VBAT=2~4.2V



6.9 Other Test

fsw = 300kHz, L = 3.3uH, RS1 = 10mR, RS2 = 5mR, COMP = 10k + 22nF	
Test Condition	Test Result
Trickle charge threshold: VBUS = 5V, Set VBAT_TARGET=4.2V	VBAT_TRCKLE=2.92V(69.5%*VBAT_TARGET)
Trickle charge current: VBUS = 5V, Set IBUS_LIM=2A	IBUS_TRCKLE=0.483A (24%*IBUS_LIM)
Charge termination current threshold: VBUS = 5V, Set IBUS_LIM=2A, EOC_SET= 0	IBUS_EOC=0.231A (11.5%*IBUS_LIM)
Recharge voltage threshold: VBUS=12V, Set VBAT_TARGET=4.2V	VBAT_RECHRG=4.01V (95.5%*VBAT_TARGET)
Battery over voltage threshold: VBUS = 5V, Set VBAT_TARGET=4.2V	VBAT_OVP=4.398 (105%*VBAT_TARGET)
VINREG voltage: VBUS=5V, Set VINREG=4.5V	VINREG=4.531V
VBAT under voltage threshold:	VBAT_UVLO=2.40V

VBUS under voltage threshold:	VBUS_UVLO=2.53V
VBUS standby current: VBUS=5V, PSTOP=3.3V, AD_START=0	I_SB_VBUS =45uA (Note: VBUS resistor divider consumes 40uA, due to VBAT flowing through body diode to VBUS)
VBUS standby current: VBUS=5V, PSTOP=3.3V, AD_START=1	I_SB_VBUS_ADC =658uA